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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,279	04/03/2001	Marcus Kuegler	CH 000007	2075

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EXAMINER	
MOISE, EMMANUEL LIONEL	
ART UNIT	**PAPER NUMBER**
2133	7

DATE MAILED: 04/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/825,279	Kuegler et al.
Examiner	**Art Unit**
Emmanuel L. Moise	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 3, 2001* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-11* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 5
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-11 are presented for examination.

Drawings

2. Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 5-7 and 8 are objected to because of the following informalities: . Appropriate correction is required.

Claim 5 should apparently read as "A method as claimed in claim 1, wherein both said loop-back and said buffering are controlled through a one-bit control signal."

Claim 6 should apparently read "A method as claimed in Claim 5, wherein signal routing between said buffering, on one hand, and test circuitry as well as core circuitry of said digital circuitry, on the other hand, are controlled through a plural bit control signal."

Claims 7 and 8 should apparently be written in independent form since their dependency upon method claims 1 and 2, respectively, does not seem to reflect Applicant's intent. For the

purposes of analyzing the claims on the merits, claims 7 and 8 will be treated as being independent.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ramamurthy et al. (U.S. Patent No. 5,787,114, hereinafter referred to "Ramamurthy).

As per claims 1 and 7, Ramamurthy teaches the claimed method/apparatus for testing digital circuitry through effecting a paired loop-back from a first buffered output to a first buffered input while within the circuitry executing at least part of the test through using a Built-In-Test methodology, characterized by effecting said loop-back from the first buffered data output to a buffered control input (See column 7, lines 15-28 and Figure 3, elements 14, 15, 16, 19, 21).

As per claims 2 and 8, Ramamurthy teaches the claimed method/apparatus for testing digital circuitry through effecting a paired loop-back from a first buffered output to a first buffered input while within the circuitry executing at least part of the test through using a Built-In-Test methodology, characterized by effecting said loop-back from a buffered control output to

the first buffered data input (See column 7, lines 15-28 and Figure 3, elements 14, 15, 16, 19, 21).

As per claims 3 and 9, Ramamurthy also teaches that the method/apparatus is characterized by effecting said loop-back from a buffered control output to the first data buffered data input (column 7, lines 25-28).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 4-6 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy (U.S. Patent No. 5,787,114).

As per claims 4 and 10, it is noted that Ramamurthy does not explicitly disclose the conversion between a digital full swing internal signal and an analog low swing external signal with respect to core circuitry of said digital circuitry. However, as mentioned by Applicant in the background of the invention, it is known in the art to convert the lows swing analog interface signals into digitally testable signals to ensure correct functionality of the interface. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to execute the claimed conversion for the purpose of ensuring correct functionality of the interface.

As per 5-6 and 11, Ramamurthy does not explicitly disclose the use of a one-bit signal to control the loop-back as well as the buffering or the routing between the buffering and test circuitry as well as core circuitry. Ramamurthy, however, discloses that a request for loop-back is asserted from off-chip to generate a loop-back test request signal (column 7, lines 18-19); thus suggesting the use of a control signal to control the loop-back test. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the claimed invention since it is known in the art that a control signal can be a single bit or a multi-bit signal. It all depends on which type of gate the signal is being provided to.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6,348,811 (Haycock et al.)

6,493,124 (Haberkorn)

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel L. Moise whose telephone number is (703)305-9763. The examiner can normally be reached on Monday - Friday from 08:30 a.m. - 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady, can be reached on (703)305-9595. Any response to this action should be mailed to: Commissioner of Patents and Trademarks Washington, D.C. 20231, or faxed to: (703) 746-7239, (for formal communications intended for entry), Or: (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Emmanuel L. Moise
Primary Patent Examiner
Art Unit 2133

April 15, 2003